Electronic Version
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Claims

[c1] 1.An integrated circuit comprising:
a device to be monitored; and
a carbon nanotube field effect transistor (CNT FET) proximate to said device to be monitored.

[c2] 2.The integrated circuit of claim 1, wherein said CNT FET is adapted to sense signals from said device to be monitored, wherein said signals comprise any of temperature, voltage, current, electric field, and magnetic field signals.

[c3] 3.The integrated circuit of claim 1, wherein said CNT FET is adapted to measure stress and strain in said integrated circuit, wherein said stress and strain comprise any of mechanical and thermal stress and strain.

[c4] 4.The integrated circuit of claim 1, wherein said CNT FET is adapted to detect defective circuits within said integrated circuit.

[c5] 5.The integrated circuit of claim 1, wherein said device to be monitored comprises a transistor configured in a metal oxide semiconductor configuration.

[c6] 6.The integrated circuit of claim 1, wherein said device to be monitored comprises:

a gate;

a source region;

a drain region; and

a gate insulator layer separating said gate from each of said source region and said drain region.

[c7] 7.The integrated circuit of claim 6, wherein said CNT FET comprises:

a CNT FET gate;

a CNT FET source region;

a CNT FET drain region; and

a carbon nanotube separating said CNT FET source region and said CNT FET drain region.

[c8] 8.The integrated circuit of claim 7, wherein said gate of said device to be monitored and said CNT FET gate comprise a shared structure.

[c9] 9.The integrated circuit of claim 7, wherein said source region of said device to be monitored and said CNT FET source region comprise a shared structure.

[c10] 10.The integrated circuit of claim 1, wherein said device to be monitored comprises any of a field effect transistor, a diode, a wire, a via, a resistor, an inductor, and a

capacitor.

[c11] 11.An integrated circuit comprising:
a primary transistor; and
an embedded carbon nanotube field effect transistor (CNT FET) spaced apart from said primary transistor, wherein said CNT FET is adapted to sense signals from said primary transistor.

[c12] 12.The integrated circuit of claim 11, wherein said signals comprise any of temperature, voltage, current, electric field, and magnetic field signals.

[c13] 13.The integrated circuit of claim 11, wherein said CNT FET is adapted to measure stress and strain in said integrated circuit, wherein said stress and strain comprise any of mechanical and thermal stress and strain.

[c14] 14.The integrated circuit of claim 11, wherein said CNT FET is adapted to detect defective circuits within said integrated circuit.

[c15] 15.The integrated circuit of claim 11, wherein said primary transistor comprises a metal oxide semiconductor configuration.

[c16] 16.The integrated circuit of claim 11, wherein said primary transistor comprises:

a gate;

a source region;

a drain region; and

a gate insulator layer separating said gate from each of said source region and said drain region.

[c17] 17.The integrated circuit of claim 16, wherein said CNT FET comprises:

a CNT FET gate;

a CNT FET source region;

a CNT FET drain region; and

a carbon nanotube separating said CNT FET source region and said CNT FET drain region.

[c18] 18.The integrated circuit of claim 17, wherein said gate of said primary transistor and said CNT FET gate comprise a shared structure.

[c19] 19.The integrated circuit of claim 17, wherein said source region of said primary transistor and said CNT FET source region comprise a shared structure.

[c20] 20.The integrated circuit of claim 11, wherein said primary transistor comprises any of a field effect transistor, a diode, a wire, a via, a resistor, an inductor, and a capacitor.

[c21] 21.A method of evaluating operating parameters of an

integrated circuit, said method comprising:
forming a primary transistor in said integrated circuit;
embedding a carbon nanotube field effect transistor (CNT FET) in said integrated circuit;
operating said primary transistor; and
detecting signals from said primary transistor using said CNT FET.

[c22] 22.The method of claim 21, wherein in said detecting, said signals comprise any of temperature, voltage, current, electric field, and magnetic field signals.

[c23] 23.The method of claim 21, further comprising measuring stress and strain in said integrated circuit using said CNT FET, wherein said stress and strain comprise any of mechanical and thermal stress and strain.

[c24] 24.The method of claim 21, further comprising detecting defective circuits within said integrated circuit using said CNT FET.

[c25] 25.The method of claim 21, wherein said forming comprises configuring said primary transistor in any of a field effect transistor, a diode, a wire, a via, a resistor, an inductor, and a capacitor configuration.